Listing of the Claims

1. (currently amended) A cooling stage for a semiconductor substrate comprising:

a pedestal having a substantially planar top surface,

a first plurality of circular grooves concentrically formed in said top surface, and

a second plurality of linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with each and ~~everyone~~ every one of said first plurality of circular grooves allowing a cooling fluid to flow therethrough when said semiconductor substrate is positioned on said top surface of the pedestal, said first plurality of circular grooves and said second plurality of linear grooves each having a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm.

2. (previously presented) A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality is at least three and said second plurality is at least two.

3. (previously presented) A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality is at least five and said second plurality is at least three.

4. (cancelled)

5. (previously presented) A cooling stage for a semiconductor substrate according to claim 1, wherein said first plurality of circular grooves and said second plurality of linear grooves each having a width between about 3 mm and about 5 mm, and a depth between about 1 mm and about 3 mm.

6. - 7. (cancelled)

8. (currently amended) A method for cooling a semiconductor substrate comprising the steps of:

providing a cooling stage comprising a wafer pedestal equipped with a grooved top surface thereon, said grooved top surface comprises a first plurality of circular grooves concentrically formed in said top surface and a second plurality of linear grooves formed in radial directions emanating from a center

of said top surface in fluid communication with each and ~~everyone~~ every one of said first plurality of circular grooves, said first plurality of circular grooves and said second plurality of linear grooves each having a width between about 1 mm and about 7 mm, and a depth between about 1 mm and about 7 mm,

positioning a heated semiconductor substrate on said grooved top surface,

flowing a cooling liquid through a cooling channel in said wafer pedestal to carry away heat transferred to said grooved top surface, and

flowing a cooling gas through said first and second plurality of circular and linear grooves to carry away heat from a backside of said heated semiconductor substrate.

9. (previously presented) A method for cooling a semiconductor substrate according to claim 8, wherein said first plurality of circular grooves comprises at least three circular grooves and said second plurality of linear grooves comprises at least two linear grooves.

10. (previously presented) A method for cooling a semiconductor substrate according to claim 8, wherein said first plurality of circular grooves comprises at least five circular grooves and said second plurality of linear grooves comprises at least three linear grooves.

11. (cancelled)

12. (previously presented) A method for cooling a semiconductor substrate according to claim 8 further comprising the step of providing said grooved top surface with a plurality of circular and linear grooves, each having a width between about 3 mm and about 5 mm, and a depth of between about 1 mm and about 3 mm.

13. (original) A method for cooling a semiconductor substrate according to claim 8 further comprising the step of positioning a semiconductor substrate exiting a high temperature sputtering chamber on said grooved top surface of said cooling stage.

14. (original) A method for cooling a semiconductor substrate according to claim 8 further comprising the step of removing a cooled-down semiconductor substrate from said cooling stage and positioning the substrate in a low temperature sputter chamber.

15. (original) A method for cooling a semiconductor substrate according to claim 8 further comprising the steps of flowing a cooling liquid through said cooling channel in said wafer pedestal, and flowing a cooling gas of an inert gas through said first and second plurality of circular and linear grooves.

16. - 18. (cancelled)

19. (currently amended) A wafer pedestal effective for cooling a high temperature processed wafer ~~according to claim 16 wherein~~ comprising:

a wafer pedestal having a substantially planar top surface,

at least three circular grooves concentrically formed in said top surface, said at least three circular grooves comprises nine circular grooves and said at least two linear grooves

comprises three linear grooves each having a width of about 2 mm and a depth of about 1 mm, and

at least two linear grooves formed in radial directions emanating from a center of said top surface in fluid communication with each and every one of said at least three circular grooves for flowing a cooling fluid therethrough cooling said high temperature processed wafer positioned thereon.

20. (previously presented) A wafer pedestal effective in cooling a high temperature processed wafer according to claim 16, wherein said cooling fluid flowing through said circular and said linear grooves is an inert gas selected from the group consisting of argon, nitrogen and helium.